

ABSTRACT OF THE DISCLOSURE

A manufacturing method of a semiconductor device having a CMOS logic circuit portion and a DRAM portion mixedly mounted on one chip. Preferably, the DRAM portion has a cylinder structure capacitor element. In the manufacturing method, the polysilicon film is formed on an interlayer film and on an inner wall of a cylinder-shaped opening formed in the interlayer film. Spherical or hemispherical grains called HSG are formed on the polysilicon film. The polysilicon film and the HSG on an upper surface of the interlayer film are removed while the polysilicon film and the HSG on the inner wall of the cylinder is retained. By performing these steps in this order, the HSG is reliably formed on the inner wall of the cylinder without fail. Therefore, a miniaturized capacitor element having high capacitance may be formed in a semiconductor device with a CMOS logic circuit portion and a DRAM portion mixedly mounted on one chip.

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